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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,188	01/31/2001	Truc Duy Nguyen	AUS920000757US1	4492

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Duke W. Yee
Carstens, Yee & Cahoon, LLP
P.O. Box 802334
Dallas, TX 75380

EXAMINER	
NGUYEN, HAU H	
ART UNIT	**PAPER NUMBER**
2676	3

DATE MAILED: 06/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,188	NGUYEN ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 19 recites the limitation "the communications unit". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 11-13, 20, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Saunders (U.S. Patent No. 5,917,497).

Referring to claims 1, 11-13, 20, and 30, Saunders teaches an algorithm is provided which is able to compute the total memory needed to store a full MIP map based on the first level that is passed to the graphics core as well as on subsequent base map level changes. Each level is then stored into the contiguous memory, if the level is valid, or in a temporary memory location, if the level is not valid. Each time the base level changes, all levels are tested for validity, and the valid levels, are placed into the contiguous memory (col. 4, lines 21-29). Saunders further teach it is first determined whether sufficient memory exists to place all of the texel data into a single block of

memory. With reference to FIGs. 2, this determination is illustrated by decision block 14. If it is not known whether there is sufficient memory, then we must compute the size of the contiguous memory block which will be needed 16, and the memory must be allocated 18 (col. 4, lines 60-66). If it is determined that sufficient memory could not be allocated 20, an error condition 22 will result. Alternatively, the base map (Level 0) values will be stored 24, and then a check is made to determine if the Level information is OK 28. By this, what is meant is that a determination is made as to whether or not the information associated with the MIP map level being loaded is consistent with the information previously known about the MIP map (col. 5, lines 13-22) (halting step in response to absence of stored texture object). Allocating memory for the next level and freeing of memory is illustrated in Fig. 4 (step 96) and Fig. 5 (steps 19, 29).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8-9, 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders (U.S. Patent No. 5,917,497).

Referring to claims 8-9, 27-28, although Saunders does not teach the removal of all stored texture objects or a single texture object in the second memory source, as cited above, Saunders does teach sufficient memory must be first allocated. Thus, depending on the size of the current texture object (once computed), the freeing (removing) of stored

texture objects for the current texture object can be a single stored texture object or all stored texture objects.

7. Claims 2, 4-7, 10, 14, 21, 23-26, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders (U.S. Patent No. 5,917,497) in view of Gannett (5,790,130).

Referring to claims 2, 4-7, 21, 23-26, as applied to claim 1 above, Saunders teaches all the limitations of claims 2, 4-7, 21, 23-26, except for the first memory source is a system memory, or assigned to a client application and the second memory source is a frame buffer, or assigned to a kernel application.

However, Gannett teaches a method for managing texture data in a texture mapping computer graphics system. The system includes a host computer with a main memory that stores texture data. A hardware device, coupled to the host computer, has a local memory that stores in blocks at least a portion of the texture data stored in the main memory at any one time. The hardware device renders texture mapped images using the texture data stored in the local memory. The method includes the following steps: monitoring the use by the hardware device of the texture data blocks stored in the local memory; tracking the priorities of the texture stored in the main memory; and replacing lowest priority and least recently used texture data blocks (texture objects used less than threshold value) in the local memory with texture data blocks needed by the hardware device to render images (col. 5, lines 67-68, and col. 6, lines 1-14). With reference to Fig. 4, Gannett teach a graphics system including a host computer 15, comprising a system memory 17, communicating with the front end board 10 for providing texture data to the texture mapping board 12 and frame buffer 14 (col. 15, lines 35-46). Gannett further teaches the determination of which block of texture data to replace in the local memory

of the hardware device when an interrupt occurs is based both on the history of usage of that block within the hardware device and the priority of the textures stored in the blocks. The prioritization of the textures is based on external user defined priorities as well as internal default priorities (col. 10, lines 59-65), thus the memory sources is assigned to either a kernel application or a client application.

Therefore, it would have been obvious to one skilled in the art to utilize the method of texture mapping as taught by Gannett in combination with the method of texture managing as taught by Saunders in order to properly managing texture memory to achieve maximum performance of the system (col. 5, lines 24-25).

Referring to claims 10 and 29, although Saunders does not teach an identifier associated with a texture object, which identifies a memory resource, Gannett teaches when the hardware driver communicates to TIM (texture interrupt manager) (as shown in Fig. 3A) that a new texture has been requested by the user, the priority of the texture and size of the texture also is communicated to TIM over the socket. TIM then provides a texture identifier to the texture, if available. At that point, a determination is made, depending on the size of the texture and number of MIP map levels of that texture, whether that texture will be stored in the shared memory location or whether that texture will be stored in TIM's own allocated system software memory location (col. 10, lines 30-39).

Therefore, it would have been obvious to one skilled in the art to utilize the method of texture mapping as taught by Gannett in combination with the method of texture managing as taught by Saunders in order to properly managing texture memory to achieve maximum performance of the system (col. 5, lines 24-25).

Referring to claim 14, as applied to claim 11 above, Saunders teaches all the limitations of claim 14 except that each memory resource has an associated texture manager for tracking allocation of memory resource.

However, as shown in Fig. 3A, Gannett teaches three separate TIMs 170, 172 and 174 (also labeled A, B, and C) communicate with the graphics hardware devices 164, 166 and 168, respectively. Each TIM is responsible for managing the storage of texture data within the local memory of the graphics hardware device to which it is connected (col. 11, lines 10-15). TIM A 170 manages the textures required by the processes PR1 and PR2 for which images are rendered by the hardware device A 164. Similarly, TIM B 172 manages the textures required by the processes PR3 and PR4 and for which images are rendered by the hardware device B 166. Finally, TIM C 174 manages the textures for the process PR5 for which images are rendered by the hardware device 168 (col. 11, lines 32-39).

Therefore, it would have been obvious to one skilled in the art to utilize the method of texture managing as taught by Gannett in combination with the method of texture managing as taught by Saunders in order to properly managing texture memory to achieve maximum performance of the system (col. 5, lines 24-25).

8. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gannett (U.S. Patent No. 5,790,130) in view of Saunders (U.S. Patent No. 5,917,497).

Referring to claims 15 and 16, Gannett teaches a method is provided for managing texture data in a texture mapping computer graphics system, wherein, as shown in Fig. 4, the system includes a texture mapping board 12 (processor unit), and a frame buffer board 14. The front end board communicates with a host computer 15 over a 52-bit bus

16. The front end board receives primitives to be rendered from the host computer over bus 16. Data representing the primitives in three dimensions then is provided by the front end board 10 to the texture mapping board 12 and the frame buffer board 14 over 85-bit bus 18 (primary bus). The texture mapping board interpolates the primitive data received to compute the screen display pixels that will represent the primitive, and determines corresponding resultant texture data for each primitive pixel. The resultant texture data is provided to the frame buffer board over a five 55-bit buses 28 (secondary bus). Thus, Gannett teaches all the limitations of claims 15 and 16, except that the processor unit allocates a first memory resource, selectively removes stored texture object in response to an inability to allocate sufficient memory, halts the allocation in response to an absence of any stored texture object, allocates in the second memory resource in response to an inability to allocate sufficient memory to the current texture object in response the halting step.

However, as cited above, Saunders teaches an algorithm is provided which is able to compute the total memory needed to store a full MIP map based on the first level that is passed to the graphics core as well as on subsequent base map level changes. Each level is then stored into the contiguous memory, if the level is valid, or in a temporary memory location, if the level is not valid. Each time the base level changes, all levels are tested for validity, and the valid levels, are placed into the contiguous memory (col. 4, lines 21-29). Saunders further teach it is first determined whether sufficient memory exists to place all of the texel data into a single block of memory. With reference to FIGs. 2, this determination is illustrated by decision block 14. If it is not known whether there is sufficient memory, then we must compute the size of the contiguous memory

block which will be needed 16, and the memory must be allocated 18 (col. 4, lines 60-66). If it is determined that sufficient memory could not be allocated 20, an error condition 22 will result. Alternatively, the base map (Level 0) values will be stored 24, and then a check is made to determine if the Level information is OK 28. By this, what is meant is that a determination is made as to whether or not the information associated with the MIP map level being loaded is consistent with the information previously known about the MIP map (col. 5, lines 13-22) (halting step in response to absence of stored texture object). Allocating memory for the next level and freeing of memory is illustrated in Fig. 4 (step 96) and Fig. 5 (steps 19, 29).

Therefore, it would have been obvious to one skilled in the art to utilize the method of texture managing as taught by Saunders in combination with the data processing system as taught by Gannet in order to reduce or eliminate memory cache misses when down-loading a fully mipped texture map down to hardware (col. 4, lines 14-16).

Referring to claims 17 and 18, as shown in Figs. 3A and 3B, Gannett teaches in one embodiment, a plurality of texture interrupt managers 1 (TIMs) (170, 172, 174) as shown in Fig. 3A, or a single TIM 176 as shown in Fig. 3B.

9. Claims 3 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders (U.S. Patent No. 5,917,497) in view of Peddada et al. (U.S. Patent No. 6,295,068).

Referring to claims 3 and 22, as cited above, Saunders teaches all the limitations of claims 3 and 22, except that the first memory source is an advanced graphics port memory.

However, Peddada et al. teach a graphics driver for an accelerated graphics port (AGP), wherein as shown in Fig. 4, application program 40 makes function call 52 to DirectX 3D graphics driver 60. DirectX 3D graphics driver 60 creates an AGP texture in AGP memory 14 when free space is not available in the local video memory. AGP memory 14 is part of the main system DRAM. DirectX 3D graphics driver 60 creates a space in AGP memory 14 for AGP texture 46 (col. 5, lines 22-28).

Therefore, it would have been obvious to one skilled in the art to utilize the method of using AGP memory as taught by Peddada et al. in combination with the data processing system as taught by Saunders in order to simplify interface between the high-level application program and the graphics driver (col. 3, lines 51-52).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892 form.

Shaw (U.S. Patent No. 6,326,975) teaches a priority method for texture map storage.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

05/27/2003

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600